Synchronous Rectification for Forward Converters

Steve Mappus
Agenda

• Synchronous Rectifier (SR) Characteristics

• Forward Converter Transformer Reset Techniques

• Forward Converter SR Gate Drive
  • Self-Driven
  • Hybrid Self-Driven
  • Control-Driven

• SR Timing Issues

• Primary-Side Trigger + Linear Predict Control (LPC)
  • Application Example
  • Measured Data
What is Synchronous Rectification?

- Replacing secondary side rectifiers (D1, D2) with MOSFETs (Q2, Q3)

Benefits of SR

- Higher Efficiency
- Lower output voltage and higher current applications benefit most
- Parallel MOSFETs for higher current

SR Nomenclature

- Q2→control SR
- Q3→freewheeling SR

Rectifier Diode Efficiency

(All Converter Losses Neglected)

\[
\eta = \frac{P_O}{P_In} = \frac{V_O \times I_O}{V_O \times I_O + V_F \times I_O} = \frac{1}{1 + \frac{V_F}{V_O}}
\]
Parallel MOSFETs

**Diode Thermal Characteristic**
- Negative temperature coefficient
- Temp increase = $V_F$ decrease
- Not easily paralleled

**SR Thermal Characteristic**
- Positive temperature coefficient
- Temp increase = $R_{DS(ON)}$ increase
- $T↑$, $R_{DS(ON)}↑$, $I_D↓$, $T↓$
- Automatic current sharing
- MOSFETs easily paralleled

Diode vs. MOSFET Thermal I-V Characteristics

$n = \text{Number parallel MOSFETs}$
Rectifier I-V Characteristics

Rectifier efficiency

\[ \eta = \frac{P_O}{P_{IN}} = \frac{V_O \times I_O}{V_O \times I_O + V_F \times I_O} = \frac{1}{1 + \frac{V_F}{V_O}} \]

Schottky Rectifier (MBR4035PT, 35V, 40A)
- Operates in first quadrant (Q1) only
- \(\eta=86.84\%, (V_F=0.5V, V_O=3.3V)\)

SR MOSFET (FDMS8670S, 30V, 42A)
- \(\eta=97.06\%, (V_F=0.1V, V_O=3.3V)\)
- >10% improvement, BUT…
  - Considers \(R_{DS(ON)}\) conduction loss only!
  - Operates in third quadrant (Q3)
SR I-V Characteristics

SR Operates in Third Quadrant

- Low current
  \[ R_{DS(Q1)} = R_{DS(Q3)} \]
- High current, SR body-diode will conduct if:
  \[ I_D \times R_{DS(ON)} \geq V_{F(BD)} \]
- For \( V_{GS}=0V \), negative current flows through SR body-diode
CCM Buck, Diode Rectification

**CCM**

\[
\frac{V_O}{V_{IN}} = D \quad P_{DI} = V_F \times I_o \times (1 - D)
\]

- D1 operates in first quadrant only – operation similar to SR
- Lower voltage converters cannot tolerate losses associated with diode rectification
DCM Buck, Diode Rectification

DCM and CCM Voltage Gain

\[ \frac{V_O}{V_{IN}} = D \]

\( k = 0.01 \)
\( k = 0.1 \)
\( k = 0.5 \)
\( k \geq 1 \)

DCM Buck Operational Waveforms

\[ \frac{V_O}{V_{IN}} = \frac{2}{1 + \sqrt{1 + \frac{4 \times k}{D^2}}} \]
where, \( k = \frac{2 \times L}{R_O \times T} \)

- D1 operates in first quadrant only – no negative current flow during DCM
- Gain is non-linear during DCM operation
Non-Isolated Synchronous Buck

SR Dominant Losses:

- Channel conduction
  \[ P_{SR(CH)} = I_O^2 \times R_{DS(ON)} \times (1 - D) \]
- Body-Diode conduction
  \[ P_{SR(BD)} = V_F \times I_O \times t_{BD} \times F_s \]
  \[ \text{Where: } t_{BD} = (t_1 - t_0) + (t_3 - t_2) \]
- Reverse Recovery
  \[ P_{SR(RR)} = Q_{RR} \times V_{IN} \times F_s \]

Dedicated Controller or Driver
- Minimize dead time
- Anti cross-conduction protection
- Optimized gate drive current
- Emulate asynchronous operation
- Reduce body-diode conduction

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SR body-diode has high $V_F$ and long $t_{RR}$!
Parallel SR Schottky Diode

Parasitic Inductance Limitation

\[
\frac{di}{dt} = \frac{V_{SR(BD)} - V_F}{L_{p1} + L_{p2}}
\]

- Typical example:

\[
\frac{di}{dt} = \frac{1.2V - 0.5V}{2 \times 5nH} = 70 \frac{A}{\mu s}
\]

- Assume 15A load current

\[
dt = \frac{15A \times \mu s}{70A} = 215ns
\]

- Current commutation time can exceed body-diode conduction time

SyncFET™ with Monolithic Schottky

- Minimal parasitic inductance
- Low \( V_F \)
- Using same example parameters:

\[
\frac{di}{dt} = 600 \frac{A}{\mu s} \text{ (measured)} \quad dt = \frac{15A \times \mu s}{600A} = 25ns
\]

- Order of magnitude improvement
SyncFET™ Reverse Recovery

FDMS7670 vs FDMS7670S SyncFET™
- SyncFET™ $Q_{RR}$ improvement of ~10%
- Previous generation trench technology would show improvement closer to ~50%
- FDMS7670S, SyncFET™ $V_F=0.43\text{V}$, FDMS7670 $V_F=0.7\text{V}$

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Forward Converter with SR

- Q2, Q3 gate drive challenges similar to synchronous buck
- Primary to secondary isolation adds additional timing requirement
- Single-ended converter topology requires transformer reset
- Optimal SR timing is related to transformer reset method
Transformer Reset Techniques

Reset Winding
  + Reset Energy Recycled
  + Simple Off-Line Solution
  - 50% Duty Cycle Limit (1:1)
  - Possible Core Saturation
  - Transformer Structure
  - Q1 Hard Switched

RCD Reset
  + Inexpensive Off-Line Solution
  + >50% Duty cycle Possible
  - Reset Energy Dissipated
  - Q1 Hard Switched

Resonant Reset
  + Reset Energy Recycled
  + Fewest Components
  + Simple Telecom Solution
  - Repeatable Design Difficult
  - High VDS Stress
  - Not for Off-Line Power
  - Not Suitable for Self-Driven SR
  - Q1 Hard Switched

Active Clamp Reset
  + High Efficiency (ZVT)
  + Higher Frequency Operation
  + Lowest Vds Stress
  + Off-Line and Telecom
  + SR Gate Drive
  - Q1, Q2 Gate Drive
  - Higher Cost
  - Limited PWM and/or Driver Choices

Reset Method Impacts Self-Driven SR Gate Drive
SR Gate Drive Methods

1. Self-Driven

2. Hybrid Self-Driven

3. Control-Driven
Self-Driven SR

- SR gate drive derived from transformer (as shown) or output inductor
- Advantages
  - Simple – no timing issues!
  - SR gate charge recycled to load
  - High efficiency with minimal components
  - Best applied to active clamp forward (D and 1-D)
Self-Driven SR (Continued)

Self-Driven SR

- Disadvantages
  - SR gate drive is not regulated
  - Not compatible with all reset techniques
  - Difficult to optimize $V_{GS}$ and $R_{DS(ON)}$ when $V_{IN} > 2:1$
    - $R_{DS(ON)}$ can vary by 10% or more
  - No control of freewheeling SR during start-up or light load
    DCM operation

$R_{DS(ON)}$ versus $V_{GS}$ for
FDMS7670AS, SyncFET™

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Hybrid Self-Driven SR

- Forward converters with resonant reset signals (ie, RCD or Resonant Reset)
- Control SR (Q2) is self-driven
- Freewheeling SR (Q3) gate-drive derived from primary-side inverted PWM
- Q1 to Q3, primary to secondary timing is critical
- Q2 to Q3 timing issues similar to non-isolated synchronous buck
Hybrid Self-Driven SR Timing

Freewheeling SR Timing Adjustments

- Split primary PWM signal
- Delay primary PWM rising edge, \( t_0 \rightarrow t_2, t_{RC1} \)
- Delay and invert secondary-side Q3 gate drive
- Apply \( t_{RC2} \) so that Q3 turns on just after VS goes negative
- Adjust \( t_0 \rightarrow t_2 > t_3 \rightarrow t_4 \) so that Q2 is OFF prior to Q3 ON (no cross-conduction for all line & load)
Advantages

- Improvement over self-driven SR
- Reduce body-diode conduction
- Regulate freewheeling SR gate drive
- Best applied to RCD or resonant reset forward converters

Disadvantages

- Non-adaptive to varying component or CCM/DCM mode change
- Control SR gate drive not regulated ($V_{GS}$ proportional to $V_{IN}$)
- Timing adjustments dependant upon R and C tolerance and duty cycle, D
- Can not be used if primary PWM includes internal gate drive
- Can not control freewheeling SR against negative current flow (DCM, pre-biased loads)

Full control of both SR MOSFETs only achievable using Control-Driven SR
Control-Driven SR

- Both SR MOSFETs are controlled by primary-side PWM
- General purpose low-side gate drivers or “smart-drivers” often used
- Offers full SR control during start-up, light-load, OCP, pre-biased output
- SR gate drive is regulated and independent of transformer reset method
- Q3 timing adjustment similar to previous Hybrid Self-Driven example
- RC Delay also needed for Q2 SR
SR secondary can be driven directly by PWM

Secondary to primary power stage propagation delay (solid arrows)
  • PWM to primary side gate drive and power transformer

Secondary to primary SR propagation delay (dashed arrows)
  • Power stage and SR delay times are often not equal
  • SR gate drive naturally leads primary MOSFET gate drive
  • Timing delay normally added in this path
Control-Driven SR Timing Delays
Primary-Side Control

Primary to secondary power stage propagation delay (solid arrows)
- PWM to primary-side gate drive and power transformer
- Delay normally added in this path

Primary to secondary SR propagation delay (dashed arrows)
- PWM to pulse transformer and SR MOSFET gate driver
- Often need to advance the SR signal (impossible)

Optimal timing adjustment requires primary and secondary sensing
Primary Sensing
- Any single-ended PWM input (SIN)
- Transformer reset voltage (DET)

Secondary Sensing
- Q2 drain-source voltage (LPC1)
- Q3 drain-source voltage (LPC2)
Primary-Side Triggering
Light Load (CCM)

FAN6210 Waveforms - Light Load (CCM), XP Triggered by DET

- XP rising edge triggers turn-on for each SR
- XN rising edge triggers turn-off for each SR
- XN triggered by PWM input (SIN) rising and falling edges
- XP control SR turn-on triggered by delayed PWM output (SOUT)
- XP freewheeling SR turn-on normally triggered by DET (shown)
Primary-Side Triggering
Full Load (CCM)

FAN6210 Waveforms - Heavy Load (CCM), XP Triggered by XN

- XP rising edge triggers turn-on for each SR
- XN rising edge triggers turn-off for each SR
- XN triggered by PWM input (SIN) rising and falling edges
- XP control SR turn-on triggered by delayed PWM output (SOUT)
- **XP freewheeling SR turn-on normally triggered by DET or XN (shown)**
  - XP can never trigger while XN is HIGH – prevents SR cross-conduction
SR Negative Current Issues

**Forward SR**
- Q2 blocks $I_{NEG}$ when Q3 turns off (Q2 off)
- $I_{NEG}$ charges SR $C_{OSS}$ during Q3 off
- $BV_{DSS}$ stress from switching $I_{NEG}$
- SR switching adjustment required (as shown)

**Synchronous Buck**
- Q1 drain clamped to DC source
- Q2 $V_{DS}$ clamped to DC source through Q1 body-diode
- Negative inductor current ok for $V_{DS}$
Linear Predict Control (LPC)

\[ \frac{1}{V_O} < \text{Ratio}_{LPC2} < \frac{1}{V_O - 0.5V} \]

- LPC Function is used to turn off Q3 before \( I_{LO}<0 \)A during DCM operation
- During CCM SR gate drive controlled by SP(XP) and SN(XN)
- SN signal follows PWM signal and cannot turn off Q3 before \( I_{LO}<0 \)
- Both SR \( V_{DS} \) monitored by resistor dividers
- Solves Problem of Negative SR Current
Primary-Side Triggering (DCM)

FAN6206 Waveforms - Light Load (DCM)
Primary-Side Triggering

Advantages
• Easily implements correct primary to secondary SR timing for forward converters
• No RC timing adjustments required
• Compatible with all forward transformer reset techniques including 2 switch forward
• Can be used with any single-ended PWM controller
• Green mode function disables freewheeling SR gate drive for $D<10\%$
• Operates in CCM and DCM
• Freewheeling SR control prevents negative current flow

Be Aware of
• SR Gate drive current limited to 0.7A/1A (source/sink)
  • Use FAN3xxx series low-side gate drivers for driving higher gate charge
• Internal fixed delays result in longer body-diode conduction times at higher frequency
  • For low output voltage converters SyncFET can help
## Primary-Side Triggering Application Circuit Specifications

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<th>90V&lt;sub&gt;AC&lt;/sub&gt;&lt;V&lt;sub&gt;IN(AC)&lt;/sub&gt;&lt;264V&lt;sub&gt;AC&lt;/sub&gt;</th>
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Intended Application: PC Power (Computing)
Why 65kHz Operation?

- Lower EMI
- Trade Off: EMI filter size versus transformer size
Primary-Side Triggering
Application Validation Circuit
Measured Waveforms
Steady State and LPC Function

SP and SN control SR switching

LPC function during DCM operation

SIN→SOUT, 300ns fixed turn-on delay

SIN→SOUT, 100ns fixed turn-off delay
Measured Waveforms
SR Dead-Time, Load Transient

FW SR↓→Control SR↑, 500ns dead-time

FW SR↑→Control SR↓, 400ns dead-time

0A→10A load transient

10A→0A load transient

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Measured Waveforms

Start-Up, OCP, Green Mode

**SR control during start-up**

**Control SR**

**Freewheeling SR**

**10A→64A overload transient**

**FW SR control during start-up**

**PWM**

(SIN)

**XP, XN**

**$V_{DS}$ Freewheeling SR**

**$V_{DS}$ Control SR**

Green mode function enabled for $D<10\%$
Measured Efficiency
Schottky vs SR

SR Efficiency Comparison
(115VAC Input, 12VDC Output, 300W, 12V/25A Output)

Efficiency (%) vs Output Power (%)

Primary-Side Trigger Control-Driven SR (FDP5800)
Schottky Rectifiers (FYP2006DN)
Summary

• Self-Driven SR
  • Best for active clamp forward where $I_{O(MIN)} > I_{LO}/2$ (BCM)
  • SR gate drive independent from primary control

• Hybrid Self-Driven SR
  • Performance improvement over self-driven SR

• Control Driven SR
  • SR timing is critical
  • Difficult to implement discretely

• FAN6210+FAN6206
  • Simplifies SR timing
  • Freewheeling SR control during DCM operation

Evaluate all SR solutions under steady state and dynamic test conditions!
Questions?

THANK YOU!
References

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